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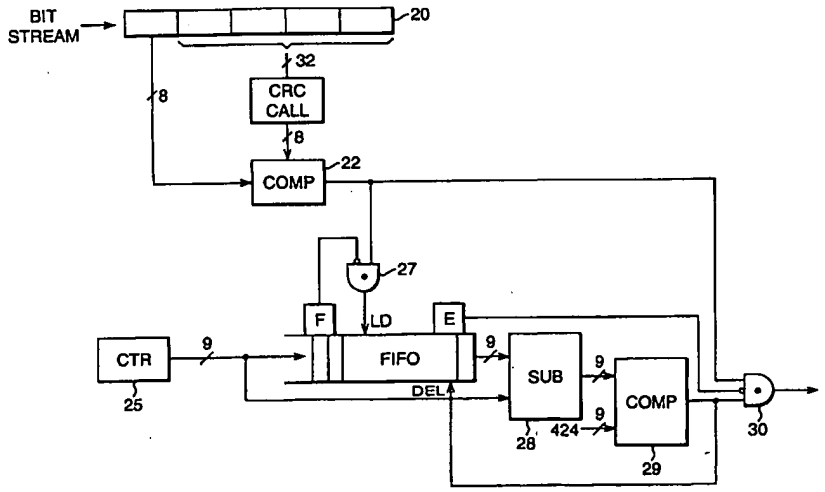

(57) Abstract

Apparatus for identifying ATM cell boundaries in a bit stream. A CRC unit (21) operates on a 40-bit (header-length) sequence of bits in a shift register (20) fed with the bit stream to calculate an HEC (header error check) function from the oldest (4) bytes of the sequence. Comparator (22) compares the result with the actual 5th byte of the sequence to detect matches. All possible 40-bit sequences are checked in this way. A FIFO memory (26) stores the position of matches over the length of a cell, in the form of time counts from a cyclic counter (25). For each match from comparator (22), a subtractor (28), comparator (29), and gate (30) determine whether there is a coincidence with a stored value in the FIFO, i.e. whether there was also a match exactly 424 bits (1 cell length) ago. To reduce the chance of spurious coincidences, further FIFOs may be connected in series and multiple coincidences detected.

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Bit Stream Synchronization

The present invention relates to bit stream synchronization, and in a preferred embodiment to the identification of cell boundaries in an ATM bit stream.

Data transmission by means of a serial bit stream is commonplace. Serial bit streams are not normally accompanied by any synchronizing information, and it is therefore necessary for the receiving unit to identify the various boundaries in the bit stream.

At the lowest level, identification of the bit boundaries may be required. This is relatively straightforward. Beyond this, however, identification of byte, word, and/or cell boundaries will also usually be required.

A specific example is in ATM (Asynchronous Transfer Mode) systems. In ATM, data is transmitted as cells. An ATM cell consists of 53 bytes, of which the first 5 bytes constitute a routing and control header and the remaining 48 bytes constitute the body. In the header, the 5th byte is a so-called HEC (Header error Control) check byte, which in fact consists of a 1 byte check value calculated from the first 4 bytes. The contents of the 48 bytes of the body are unconstrained.

With a continuous stream of ATM cells, therefore, it is necessary to identify the cell boundaries. Once that has been achieved, the interior structure of the cells (division between header and body, and division into bytes) can be readily achieved.

Cell boundary identification is conventionally performed by monitoring the bit stream for a 40-bit (5 byte) sequence which has the header structure, ie in which the value in the 5th byte matches the HEC value calculated for the preceding 4 bytes.

Monitoring

It is, however, possible for such a structure to occur by chance in the bit stream, as will be explained. The 8-bit HEC has one of 256 possible values. Thus,

for a random pattern of 40 bits, there is a one in 256 chance that the HEC calculated for the first 32 bits will match the value contained in the next 8 bits. This is, of course, relatively low. However, each cell contains 53 bytes (424 bits), so the chance of a false match occurring within an entire cell (which provides 424 possible match points) is relatively high; simplistically the chance of finding no false match is $(255/256)^{424}$, which is only about 20% or in other words there is an 80% chance of at least one false match at some point in the cell. (In fact, the above is a simplification; due to the nature of the algorithm, the probability of finding adjacent false matches is less than if the likelihood of a false match were 1/256 in each case. Also, the simplification does not take into account the possibility of bit errors occurring in transmission).

Thus, the detection of a 40-bit sequence with the header structure is therefore regarded as indicating only a provisional or potential cell header. A true cell header will be followed by further cell headers at intervals of 53 bytes, ie 424 bits. So to improve the reliability of the check whether a potential cell header is a true cell header, the bit stream is inspected at intervals of 424 bits to determine whether the 40-bit sequence at each interval also has the cell header structure. The likelihood of two false matches at exactly 424 bit intervals is much lower than that of a single false match. (If desired, further inspections of the bit stream at further intervals of 424 bits can be made, to decrease the probability of false coincidences to any desired degree.) If the 40-bit sequence following the first interval does not have the correct header structure, then it can be assumed that the original potential cell header was not a true cell header, and the bit stream must be monitored for a further potential cell header.

Once two (or the desired number) of sequential matches have been detected, synchronisation with the bitstream can be established, and known processing techniques can be applied to the bitstream.

Detection of the start of an ATM cell by verifying HEC values for two sequential cells is a known problem, and has been solved in the prior art. However, prior art methods have generally required large arrays of logic gates which are capable

of processing widely separated regions of the bitstream simultaneously. US-A-5570368 discloses a cell multiplexer wherein time division multiplex data is stored in a central buffer memory prior to being output as ATM cells through a cell interface. A cell delineation function is required for each input stream so that cell boundaries can be identified. A cell delineation mechanism is disclosed whereby the state of each line is stored in a common memory. WO-A94/00940 discloses a device for ATM cell synchronisation, but it depends entirely on coprimality of a header and payload as a way to reduce the possible number of matches that need to be made in determining cell boundaries. This coprimality allows non-overlapping but "substantially" continuous blocks of cells to be differentiated. The present invention does not rely on coprimality.

One object of the invention is to provide an improved technique for detecting cell boundaries or establishing synchronisation with a bit stream. Although primarily applicable to delineation of ATM cells, the invention may be more generally applied to detect the sequential occurrence of two or more "signatures" at predetermined intervals in a serial bit stream. At least in preferred embodiments of the invention, cell delineation can be performed with considerably few logic gates than was possible with prior art techniques.

Features of the invention are defined by the attached claims.

According to an embodiment of the invention, when a signature match is detected, an indicator of its position is registered in memory and compared to the position of a subsequently detected match. Thus, the portion of the bit stream which originally triggered the match need not be present (although the bit stream may be stored for other purposes) when the second match is detected. Therefore, the apparatus does not need lengthy shift registers to hold large portions of the bit stream while detection is carried out. Whilst the signature match can be detected by comparing the received bit stream with one or more predetermined explicitly set bit patterns, it is preferable if the pattern comprises a relationship between portions of the

sequence. Thus the signature verification means is preferably arranged to calculate a signature function (preferably a Header Error Correction or Cyclic Redundancy Check function) from a first part of the sequence and to compare the result with the contents of a second part of the sequence. Although typically the first and second parts will be contiguous, it is possible for them to be separated by portions of bitstream which do not feature in the signature verification process.

It will be appreciated that the absolute value of the positional indicator is unimportant provided that its relationship to a desired portion of the sequence, for example the start of the cell concerned or the next cell, is known or can be determined.

Ideally, the apparatus includes a counter, the value of the counter being incremented as the bitstream passes through the apparatus, the positional indicator being derived from the counter. This provides a convenient means of providing positional indicators.

The counter most preferably has a maximum value at least equal to said predetermined spacing. This enables reliable detection of matches at the desired spacing, without problems of false detection at "alias" positions (although this may be tolerated in certain cases; the probability of false detection will still be significantly lower than in the case of matching only a single signature).

However it is found that the counter maximum value or cycle length need not be exactly equal to the predetermined spacing (if it is equal, this is advantageous, as two matches separated by the predetermined spacing will have equal counter values; in such a case, the determining means need simply compare the present (or later) counter value to the earlier stored counter value). Nor need the counter maximum value be sufficiently large to ensure that all values are unique, without the counter resetting while attempting to establish synchronisation (although this also has advantages; the detecting means need simply detect a difference in later and earlier

counter values equal to the spacing). Instead, it has been appreciated that a counter which has a maximum value greater than the spacing but not necessarily related to the spacing may be employed, provided detection of the difference in counter values employs arithmetic modulo the maximum counter value.

Preferably the counter is an n-bit binary counter, where 2^n is greater than or equal to the predetermined spacing, preferably the next power of 2 above the predetermined spacing (for example, a 9 bit counter can be employed to detect ATM cell headers having a spacing of 424 bits). This has a particular advantage; when a binary adder or subtracter (which can conveniently be implemented in hardware using relatively few gates) is employed to determine a difference in spacing from two n-bit counter values, the result will automatically account for wraparound of the counter if only an n-bit result is employed.

In the case of ATM cell delineation, the detection will be used to match header values in a cell to the corresponding HEC byte. However, in some cases, different signature verification algorithms may be employed; a first check may be performed to detect a cell header and a second check may be performed to detect a data portion, and where both matches are detected at the expected spacing, the cell can be identified in this way.

The predetermined spacing is preferably equal to the cell length, 424 bits in the case of an ATM cell of 53 bytes.

The detecting means may be arranged to detect the predetermined spacing based on stored positional data, for example by scanning the memory contents, the detecting means thus operating after positional indicators have been stored in memory. Most preferably, however, the detecting means is arranged to receive the (current) output of the signature verification means (without substantial delay) and to detect the predetermined spacing based on a previously stored positional indicator and an indicator of the present position (or the position in the bitstream to which the output of the signature verification means relates). In this way, detection speed is enhanced,

and the circuitry may in fact be simplified.

In the specific case of ATM cell identification, the sequence length is the header length of 40 bits. The signature function is a defined HEC algorithm, and is calculated from the first 32 bits of the sequence; this is then compared with the last 8 bits of the sequence.

The memory preferably consists of a FIFO memory for receiving positional indicators, preferably coupled to a cyclic counter which counts the bits of the bit stream. Each count at which a match is signalled is entered into the input end of the FIFO register, and is preferably deleted from its output end when the counter counts on beyond the stored count by more than the predetermined spacing.

The size of the FIFO register is preferably substantially less than the predetermined spacing. In the case of ATM, the chance of a random or false match in a single sequence is roughly 1 in 250. Over 424 bits (ie a cell length) of the bit sequence, there will therefore usually be a single false match, and quite often 2 false matches, with the chance of more false matches decreasing rapidly. Surprisingly, a FIFO length of less than 1/10th the number of bits in the spacing, even less than about 1/32 the number of bits is normally sufficient. A FIFO length of 10 is sufficient to reduce the chance of FIFO overflow and consequent failure to detect a cell start in 1 cell time to less than about 1 in 10^6, and about 12 words is likely to be sufficient for all practical purposes. In the event of a fresh entry to the FIFO arriving when the FIFO is full, to prevent overflow either the oldest entry can be prematurely deleted or the entry of fresh values can be inhibited. In general, inhibition of the entry of fresh values is preferred, as this prevents entries being deleted from the FIFO before the predetermined spacing has been reached.

It can be seen that the product of the number of bits in the FIFO (for example 9) and the length of the FIFO (for example 10 words) may be less than the number of bits in the interval between signatures (this is, in general, a preferred feature). This can lead to a saving in substrate space required to implement the hardware as

compared to conventional techniques.

If the detection of more than 2 coincidences is desired, then further FIFO registers can be provided, connected in series. Such further FIFO registers can be shorter than the first FIFO register, because most of the values stored in the first FIFO register will not result in coincidences and so will not be passed on to the second, and so on.

As an alternative to a FIFO, the memory for storing the matches may be a shift register whose length is the same as the cell length, with a bit being entered into the shift register each time there is a match. In such a case, the positional indicator is stored as the position of the bit in the shift register. Each time the monitoring means detects a match, its output is effectively ANDed with the output of the shift register. A 1 coming from the shift register indicates that there was a match exactly one cell length previously, and a coincidence of a current match and a stored match can therefore be taken as indicating that a true cell boundary has been detected.

Apparatus for identifying cell boundaries in an ATM bit stream will now be described, by way of example, with reference to the drawings, in which:

Fig. 1 is a diagram of the structure of an ATM bit stream;

Fig. 2 is a block diagram of a first embodiment of the apparatus;

Fig. 3 is a block diagram of a second embodiment of the apparatus.

Fig. 1A shows a bit stream consisting of a series of ATM cells 10, 11, 12, etc. The arrow indicates the direction of the bit stream; cell 10 is the oldest (the first cell transmitted and received), cell 11 is the cell transmitted immediately after cell 11, and so on, with cell 13 being the youngest (most recently transmitted).

Fig. 1B shows the cell 10 expanded into a header 10H and a body 10B; Fig.

1C shows the header 10H expanded into 5 bytes HB1 to HB5; and Fig. 1D shows the byte HB5 expanded into 8 bits. The first four bytes HB1 to HB4 of the header contain routing and other information about the cell; the 5th byte HB5 is a check value, which is calculated from the first 4 bytes HB1 to HB4 of the header. This byte is known as the header error control (HEC). The body 10B is in fact 48 bytes long, so the total cell length is 53 bytes, ie 424 (53 x 8) bits.

The purpose of the present apparatus is to identify the points in the bit stream shown in Fig. 1A where the ATM cell boundaries lie. There are 424 possible positions for the cell boundaries, only one of which is correct.

Referring to Fig. 2, in a first embodiment, the incoming bit stream is fed into a 40-bit shift register 20, which therefore holds in succession all 40-bit sequences in the bit stream. The first 4 bytes of this shift register feed a CRC calculation circuit 21, which feeds a comparator 22. The last byte of the shift register 20 (ie is the one which will contain the most recent 8 bits from the bit stream) also feeds the comparator 22. The comparator 22 thus detects a match between the CRC calculated from the first 4 bytes in the shift register and the contents of the 5th byte. A match indicates that the sequence in the shift register is a potential header.

The CRC calculation circuit 21 is preferably designed to operate with high parallelism, and we will assume that it generates its (8-bit) output virtually instantaneously. In practice, however, it may operate on a cascade or pipeline principle, with the output appearing after some delay, with several CRC calculations proceeding through their respective stages in the calculation circuit at the same time. In this case, a corresponding delay must be provided in the path from the 5th byte in the shift register 20 to the comparator 22.

There is a counter 25, which counts in synchronism with the bit rate of the bit stream entering the shift register 20. The counter 25 has 9 bits, so its cycle length is 512, which is the next power of 2 above the cell length of 424 bits. The output of this counter is provided as input data to a FIFO register 26. The output of the

comparator 22 is fed to the load control input of the FIFO 26, so that each time the comparator 22 detects a match, ie a potential ATM header, the count of the counter 25 is loaded into the FIFO 26. (The comparator 22 feeds the FIFO 26 via a gate 27 which receives an inhibit signal from "full" control output F of the FIFO. Thus if the FIFO is full, any further counts from the counter 25 are lost until more room is created in the FIFO by some counts being deleted from it, as discussed below.)

A subtracter 28 is fed with the oldest count in the FIFO 26 and the current count from the counter 25, and produces the difference between those two values. The subtracter 28 feeds a comparator 29 which also has a fixed input of the value 424. This comparator therefore produces a true output when the difference from the subtracter 28 is 424. (More precisely, the comparator detects when the output of the subtractor is either 424 or 424-512, ie -88. It does this merely by ignoring the sign bit in the subtractor output.)

It is evident that the output of the comparator 29 reproduces the output of the comparator 22 with a delay of 424 bits, ie a delay of 1 ATM cell. The outputs of the two comparators 22 and 29 are fed to an AND gate 30 which detects any coincidence. Such a coincidence indicates that two potential ATM headers have been detected exactly 1 cell length apart, and this is taken as indicating that true cell headers have been detected.

The comparator 29 also feeds the delete control input of the FIFO 26. As soon as the output (oldest count) in the FIFO 26 becomes more than 424 bits old, it is deleted from the FIFO. Thus, data remains in the FIFO for no more than 1 cell length; this prevents spurious detection caused by previously stored values.

The FIFO 26 also has an "empty" control output E, which is fed as an inhibit signal to the coincidence gate 30. This prevents a coincidence being detected when the FIFO is empty. (This situation will in general only occur if there has been some error, for example due to a corrupted bit stream, or on initialisation of the apparatus, since matches from the comparator 22 should occur at least every 424 bits.)

The system as described so far detects double matches. If it is desired to detect triple matches, a further FIFO can be provided, loaded with the output of the FIFO 26 when the gate 30 detects a coincidence, and feeding a further subtractor (also fed from the counter 25), comparator (fed with a fixed value of 336, ie 424 x 2 modulo 512), and coincidence gate (fed also from the comparator 22).

A second embodiment will now be described, with reference to Fig. 3. Similar functional elements to those of the first embodiment will not be described further. In this embodiment, the FIFO contains additional match counter bits, for counting the number of sequential matches at the predetermined spacing (in a simplification, a single flag bit may be used to detect three consecutive matches). The match counter bits (or single flag bit) associated with a first counter value are initially set to a predetermined value (for example 0) when a first match is first detected. However, if a subsequent match is detected at the predetermined spacing after the first match, the match counter bits are incremented by incrementer 50 and the new counter value and match counter bits stored in the FIFO. Then, if a match is detected at a predetermined spacing after a stored counter value, by detecting the value of the match counter bits in a further comparator 52, a desired number of matches can be identified. (If a single flag bit associated with the stored counter value for the previous match is set, it is possible to determine that a third sequential match has been detected directly from the flag bit). The technique can readily be extended by providing more counter bits, and incrementing the associated counter values on each detection of a match. Thus an 11 bit wide FIFO can provide 2 counter bits, enabling detection of up to 5 successive matches (the last match detected need not be stored, and it is to be remembered that a counter value of 0 corresponds to the first match). In such a case, the FIFO may need to be longer than a FIFO which only stores single matches. However, since the likelihood of 2 or more false matches is generally small, it will not normally be necessary to add more than a few extra words for each additional match to detect.

In summary, a preferred embodiment of the invention includes apparatus for identifying cell boundaries in an ATM bit stream of cells. The apparatus comprises

cell boundary identification means for receiving the ATM bit stream and for identifying a bit sequence in the stream which signifies a cell boundary, a match signal being generated when a potential cell boundary is identified. Memory means are provided which respond to the match signals each time a cell boundary is identified. The memory means is synchronised with the bit rate of the data stream so as to store data which represents the position of the identified potential cell boundary in the bit stream, and it is also arranged to achieve synchronisation when a predetermined number of match signals have been detected with the same cell boundary spacing.

The memory means can store a respective bit stream count in response to each match signal and then compares the spacing between consecutive bit stream counts with a predetermined bit spacing between the cell boundaries, whereby synchronisation is achieved only when said spacings match. In this case, the memory means can include coincidence means responsive to coincidence of a current match signal with consecutive stored match signals to generate a synchronisation signal.

Alternatively, the memory means can include counter means for counting match signals with a similar predetermined bit spacing and for achieving synchronisation when a predetermined number of said similar match signals have been counted.

These preferred arrangements are particularly suitable for dealing with cells that each have a header which includes routing bytes and an HEC check byte, wherein the cell identification means identifies the cell boundary by calculating the value of the routing bytes, comparing the calculated value with the HEC check byte and then generating the match signal when the calculated value matches the HEC check byte.

A method is also disclosed of achieving synchronisation in a bit stream of cells with no defined synchronisation pattern, each cell having a header portion and a data portion. More particularly, the method includes the steps of identifying a bit sequence in the stream which signifies a cell boundary; generating a match signal each time a potential cell boundary is identified; storing data, which is synchronised with the bit rate of the data stream and which represents the positions of the potential cell

boundaries; and establishing synchronisation when a predetermined number of match signals have been detected with the same cell boundary spacing.

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Claims

1. Apparatus for identifying predetermined points in a bit stream, comprising:

signature verification means arranged to receive a sequence of bits from the bit stream and to signal a signature match if the sequence of bits conforms to a predetermined pattern;

a memory for storing positional indicators of signature matches (if any) detected as the bitstream passes through the signature verification means; and

means for detecting, based on the stored positional indicator of at least one previously detected signature match, the occurrence of bit patterns having a predetermined signature at two (or more) positions in the bitstream having a predetermined spacing.

2. Apparatus according to Claim 1, wherein the signature verification means is arranged to calculate a signature function from a first part of the sequence and to compare the result with the contents of a second part of the sequence.

3. Apparatus according to claim 1 or 2 wherein the signature function is a header error control (HEC) or a CRC function.

4. Apparatus according to any preceding claim wherein the memory for storing the matches is a FIFO memory coupled to a cyclic counter which counts the bits of the bit stream.

5. Apparatus according to claim 4 wherein the cycle length of the counter is the same as the predetermined spacing.

6. Apparatus according to claim 4 wherein the cycle length of the counter is a power of two, preferably the next power of 2 greater than the predetermined spacing.

7. Apparatus according to any of Claims 3 to 6 arranged to discard the first entry in the FIFO when the difference between the current counter value and the stored counter value equals the predetermined spacing.

8. Apparatus according to any one of claims 4 to 7 wherein the length of the FIFO register is substantially less than the cell length.

9. Apparatus according to any one of claims 4 to 8 arranged so that, in the event of the FIFO becoming full, the entry of fresh values into the FIFO is inhibited.

10. Apparatus according to any preceding claim arranged to establish synchronisation with an ATM cell stream, wherein said predetermined spacing equals an ATM cell length of 424 bits.

11. Apparatus according to and of claims 4-9, wherein the FIFO length is about 16 words or less, preferably about 10 words or less.

12. Apparatus according to any previous claim including further means for detecting a third or subsequent signature match.

13. Apparatus according to Claim 12, wherein the further means includes further memory means for storing an identifier of positions at which a second signature match has been detected.

14. Apparatus for identifying cell boundaries in an ATM bit stream of cells, wherein each cell has a header portion and a data portion, the apparatus comprising:

cell boundary identification means for receiving the ATM bit stream and for identifying a bit sequence in the stream which signifies a cell boundary, a match signal being generated when a potential cell boundary is identified;

memory means which respond to the match signals each time the potential cell boundary is identified; the memory means being synchronised with the bit rate of the data stream so as to store data which represents the position of the identified potential cell boundary in the bit stream; and the memory means also being arranged to achieve synchronisation when a predetermined number of match signals have been detected with the same cell boundary spacing.

15. Apparatus according to claim 14, wherein the memory means stores a respective bit stream count in response to each match signal and then compares the spacing between consecutive bit stream counts with a predetermined bit spacing between the cell boundaries, whereby synchronisation is achieved only when said spacings match.

16. Apparatus according to claim 15, wherein the memory means includes coincidence means responsive to coincidence of a current match signal with consecutive stored match signals to generate a synchronisation signal.

17. Apparatus according to claim 14, wherein the memory means includes counter means for counting match signals with a similar predetermined bit spacing and for achieving synchronisation when a predetermined number of said similar match signals have been counted.

18. Apparatus according to any of claims 14-17, wherein each cell has a header which includes routing bytes and an HEC check byte, and wherein the cell identification means identifies the cell boundary by calculating the value of the routing bytes, comparing the calculated value with the HEC check byte and then generating the match signal when the calculated value matches the HEC check byte.

19. A method of achieving synchronisation in a bit stream of cells with no defined synchronisation pattern, wherein each cell has a header portion and a data portion, the method including the steps of:

identifying a bit sequence in the stream which signifies a cell boundary;

generating a match signal each time a potential cell boundary is identified; and

storing data, which is synchronised with the bit rate of the data stream and which represents the positions of the identified potential cell boundaries; and

establishing synchronisation when a predetermined number of match signals have been detected with the same cell boundary spacing.

FIG. 1

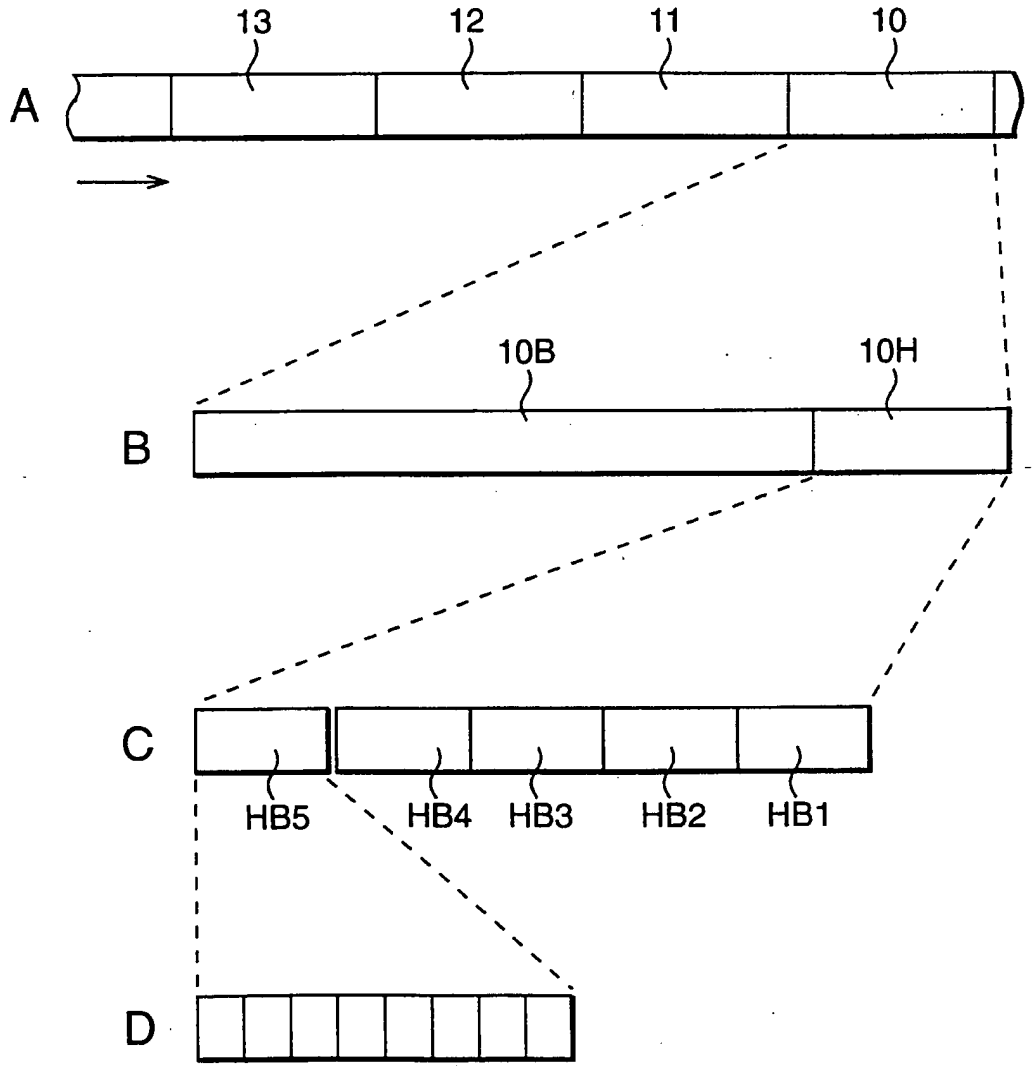
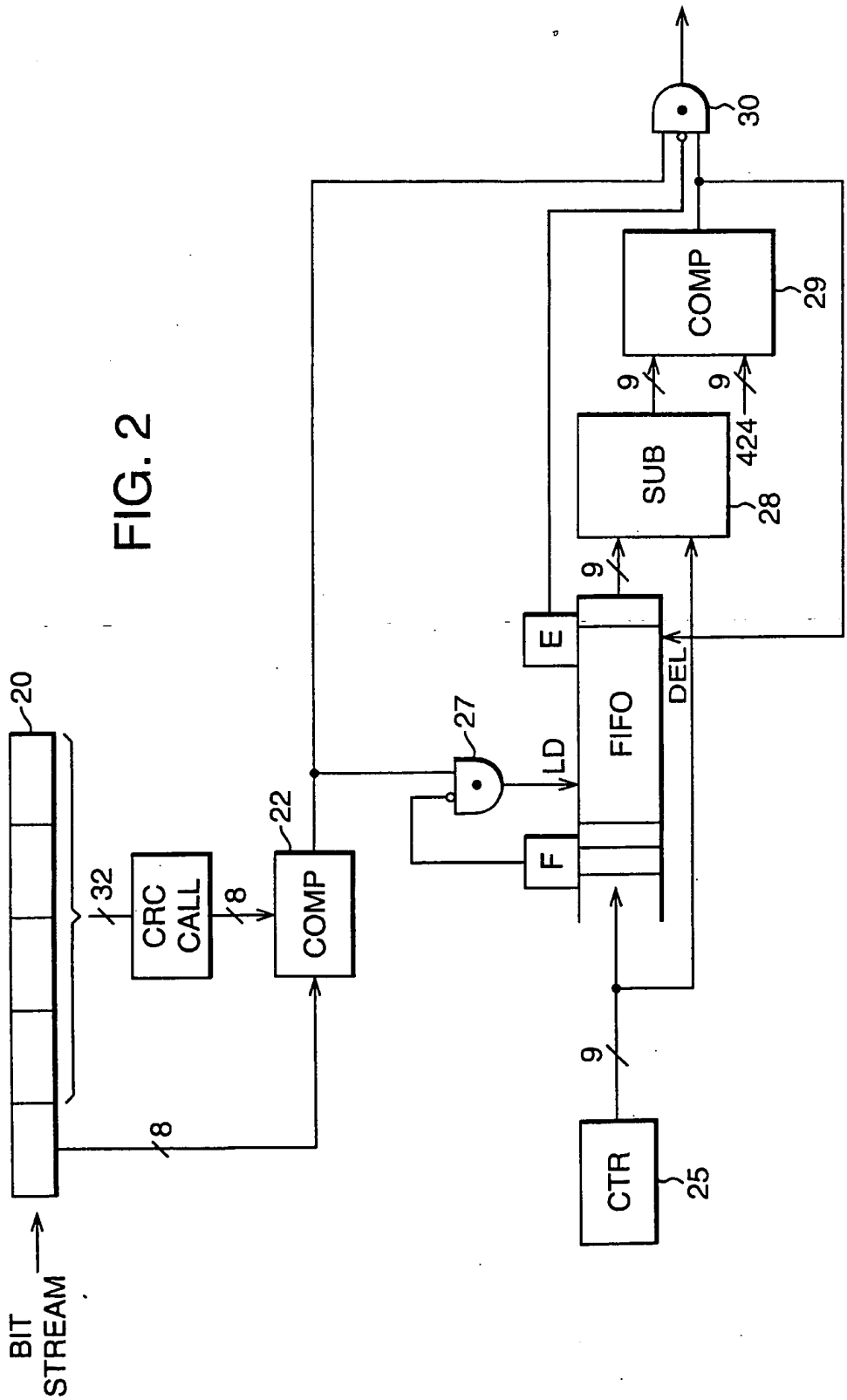


FIG. 2



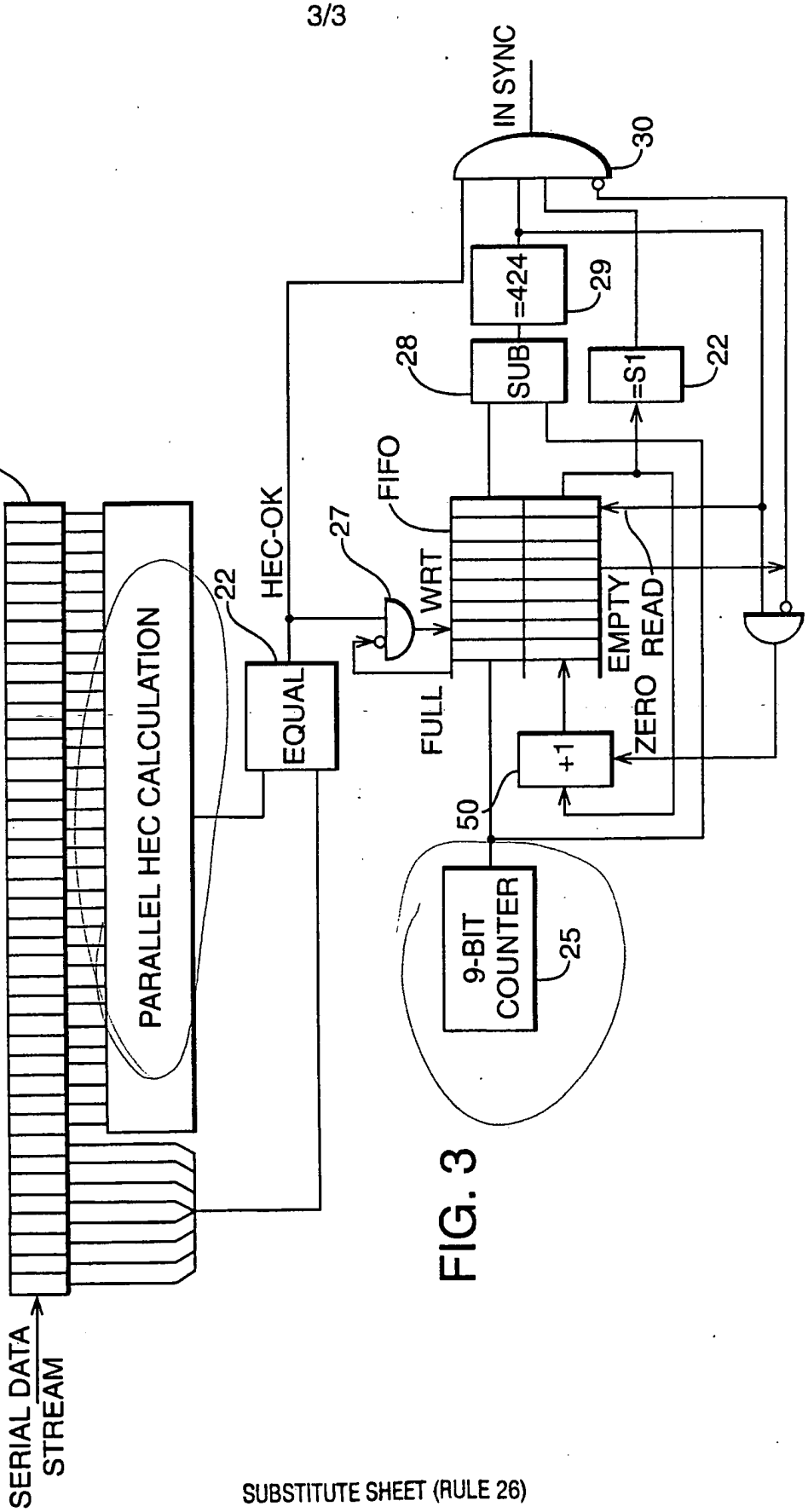


FIG. 3

INTERNATIONAL SEARCH REPORT

In tional Application No
PCT/GB 98/03376

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/04 H04L7/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 579 324 A (BUHRGARD KARL S M) 26 November 1996 see column 1, line 14 - line 17 see column 3, line 33 - line 54 see column 4, line 61 - column 7, line 18; claims 1,4 ---	1,3,12, 14,19
A	DODDS D E ET AL: "ATM FRAMING USING CRC BYTE" SERVING HUMANITY THROUGH COMMUNICATIONS. SUPERCOMM/ICC, NEW ORLEANS, MAY 1 - 5, 1994, vol. 1, 1 May 1994, pages 410-414, XP000438949 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see page 410, column 2, line 18 - line 28; figure 2 --- -/--	2

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
5 February 1999	15/02/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gregori, S

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 98/03376

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 503 667 A (FUJITSU LTD) 16 September 1992 see column 6, line 18 - column 7, line 15 see column 11, line 29 - column 12, line 35 -----	1-19

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/GB 98/03376

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